CBCS SCHEME

USN | | | | | | | | | | | **15EC655**

Sixth Semester B.E. Degree Examination, Feb./Mar. 2022
Microelectronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain channel length modulation. Obtain the modified equation of drain current in saturation region operation of MOSFET. **(07 Marks)**

b. Write a note on body and temperature effects observed in MOSFETs. **(05 Marks)**

c. An enhancement PMOS transistor has $K_p^1(W/L) = 80\mu A/V^2$, V_t = -1.5V and λ = -0.02V^{-1}. The gate is connected to ground and the source to +5V. Find the drain current for V_D = +4V. **(04 Marks)**

OR

2 a. For the common source circuit shown in Fig.Q.2(a), sketch the transfer characteristic and obtain analytical expressions for the same. **(08 Marks)**

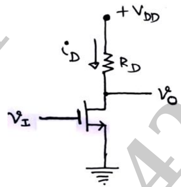

Fig.Q.2(a)

b. An n-channel enhancement MOSFET is measured to have a drain current of 4mA at $V_{GS} = V_{DS}$ = 5V and of 1mA at $V_{GS} = V_{DS}$ = 3V. What are the values of $K_n^1(W/L)$ and V_t for this device? **(04 Marks)**

c. For the circuit shown in Fig.Q.2(c), what should be the value of R_D to establish a drain voltage of 0.1V? What is the effective resistance between drain and source at this operating point? Let V_t = 1V and $K_n^1(W/L) = 1mA/V^2$. **(04 Marks)**

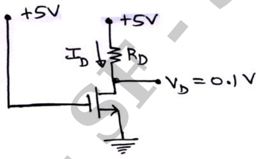

Fig.Q.2(c)

Module-2

3 a. Consider the MOSFET circuit shown in Fig.Q.3(a). Derive an expression for MOSFET trans conductance parameter, g_m. Also, show how g_m can be obtained from the transfer characteristic of the device. **(06 Marks)**

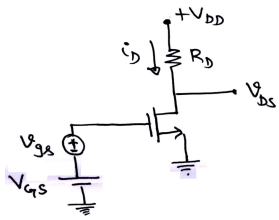

Fig.Q.3(a)

b. Derive the expression of higher cut-off frequency for a common source amplifier circuit. **(08 Marks)**

c. In a MOS amplifier circuit, for a particular value of I_D (DC bias current), the value device g_m is found to be 0.75m A/V. If I_D is increased by 4 times, what will be the new value of device g_m. **(02 Marks)**

OR

4 a. Design the biasing circuit shown in Fig.Q.4(a) to establish a drain current, $I_D = 0.5mA$. The MOSFET has $V_t = 1V$, $K_n^1\left(\frac{W}{L}\right) = 1mA/V^2$ and $V_{DD} = 15V$. Assume one-third of V_{DD} across R_D and R_S, and neglect channel length modulation, $\lambda = 0$. Determine percentage change in value of I_D when MOSFET is replaced by another having $V_t = 1.5V$. **(09 Marks)**

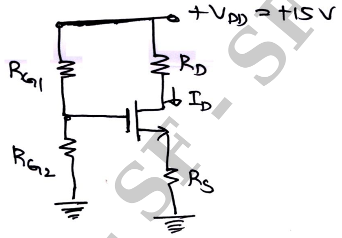

Fig.Q.4(a)

b. Obtain T-model for a MOSFET from its hybrid-II model. **(04 Marks)**

c. For an n-channel MOSFET with $t_{ox} = 10nm$, $L = 1\mu m$, $W = 10\mu m$, $L_{ov} = 0.05\pi m$ and $C_{sbo} = C_{dbo} = 10fF$. Find the values of C_{ox}, C_{ov} and C_{gs}. Note that permittivity of oxide, $\varepsilon_{ox} = 3.9\varepsilon_o$. **(03 Marks)**

Module-3

5 a. Consider a source follower circuit. Let $R_{sig} = 1M\Omega$, $R_L = 15K\Omega$, $R_G = 4.7M\Omega$, $g_m = 1m\mho$ and $r_o = 150K\Omega$. Find R_{in}, A_V, R_{out} and G_V of the circuit. **(06 Marks)**

b. Explain MOSFET current steering circuit. **(07 Marks)**

c. Mention the effects of using source resistance, R_S, in a common source amplifier circuit. **(03 Marks)**

OR

6 a. Derive the approximate expression for upper cut off frequency (3dB) for the direct coupled IC amplifier in the case of absence of dominant pole. **(06 Marks)**

b. Compare BJT and MOSFET with respect to transconductance, g_m and output resistance, r_o. **(04 Marks)**

c. Obtain the value of R in the circuit of Fig.Q.6(c) for $V_{DD} = 3V$ and $I_{REF} = I_o = 100\mu A$. Let Q_1 and Q_2 be matched, channel lengths = $1\mu m$, channel widths = $10\mu m$, $V_t = 0.7V$ and $K_n^1 = 200\mu A/V^2$. Assuming early voltage parameter, $V_A^1 = 20V/\mu m$, find the output resistance of the circuit. Also, find the lowest possible value of V_o. **(06 Marks)**

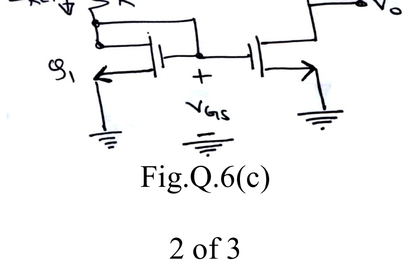

Fig.Q.6(c)

Module-4

7 a. A CMOS common-source amplifier has W/L = 7.2μm/0.36μm for all transistors, μ_nC_{ox} = 387μA/V^2, μ_pC_{ox} = 86μA/V^2, I_{REF} = 100μA, $V^1_{An} = 5V/\mu m$ and $|V^1_{AP}| = 6V/\mu m$. For Q_1, C_{gs} = 20fF, C_{gd} = 5fF, C_L = 25fF and R_{sig} = 10KΩ. Assume that C_L includes all the capacitances introduced by Q_2 at output node. Find upper 3dB frequency, using open-circuit time constants. **(08 Marks)**

b. For a common-gate amplifier with an active load, derive the expressions for R_{in}, A_v and G_v. **(08 Marks)**

OR

8 a. Derive the expressions of R_{out} and A_{vo}, for a cascade amplifier with active load. Also, draw the equivalent circuits at the output of a cascade amplifier. **(08 Marks)**

b. Sketch the high frequency equivalent circuit of common gate amplifier with active load. Using the same, derive an expression of f_H of the circuit using open-circuit time constants method. **(08 Marks)**

Module-5

9 a. Obtain an expression of CMRR resulting from g_m mismatch in a MOS differential pair circuit. **(08 Marks)**

b. Explain the operation of two stage CMOS OP-AMP and hence determine DC open-loop gain. **(08 Marks)**

OR

10 a. Sketch the active loaded MOS differential pair circuit and hence determine, short circuit transconductance parameter, G_m. **(08 Marks)**

b. For the MOS differential pair with a common-mode voltage, V_{CM} applied, as shown in Fig.Q.10(b), find V_{OV}, V_{GS}, i_{D_1}, i_{D_2}, V_{D_1}, V_{D_2} and V_s. What is the highest value of V_{CM} for which Q_1 and Q_2 remain in saturation? If current source I requires a minimum voltage of 0.4V to operate properly, what is the lowest value allowed for V_{CM}. Let $V_{DD} = V_{SS}$ = 1.5V, $K^1_n\left(\frac{W}{L}\right)$ = 4mA/V^2, I = 0.4mA and R_D = 2.5KΩ. Assume the transistors are matched. Given V_t = 0.5V. **(08 Marks)**

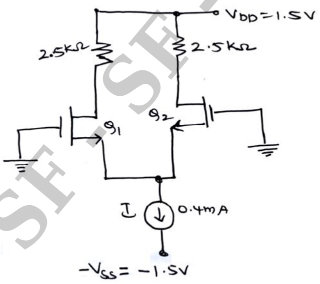

Fig.Q.10(b)

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